Institute of Geophysics

ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

LISA GRS FRONT-END ELECTRONICS CHARACTERIZATION

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First eLISA Consortium,
October 22-23, 2012

LTP – GRS

LISA Technology Package Inertial Sensor Front-End Electronics (IS FEE)

ETH Zurich	*Principal Investigator*	*Domenico Giardini*
	Engineering Team:	*Davor Mance, Peter Zweifel*
University of Zurich	*Co-Investigator*	*Philippe Jetzer*

- *ETH in charge of IS FEE since 2003*
- *Swiss funding via ESA Prodex*
- *The flight hardware was developed by RUAG Space Zurich, with HES-SO as subcontractor (HES-SO = University of Applied Sciences Western Switzerland)*

GRS FRONT END ELECTRONICS CHARACTERIZATION FOR LISA

- *ESA Project*
- *Funding by ESA via Core Technology Programme and Special Initiative*
- *ESA contracted RUAG Space with ETH and HES-SO as subcontractors*
- *Kicked-off in April 2011, expected overall duration 2.5 years*

GRS PROJECT

Project Objective

- *GRS front-end electronics (FEE) shall fullfil LISA requirements*
- *The residual acceleration required by LISA must be a factor 10 better than that required of LISA Pathfinder*
- *Building a FEE breadboard, including redundacy switching, but nominal configuration only*

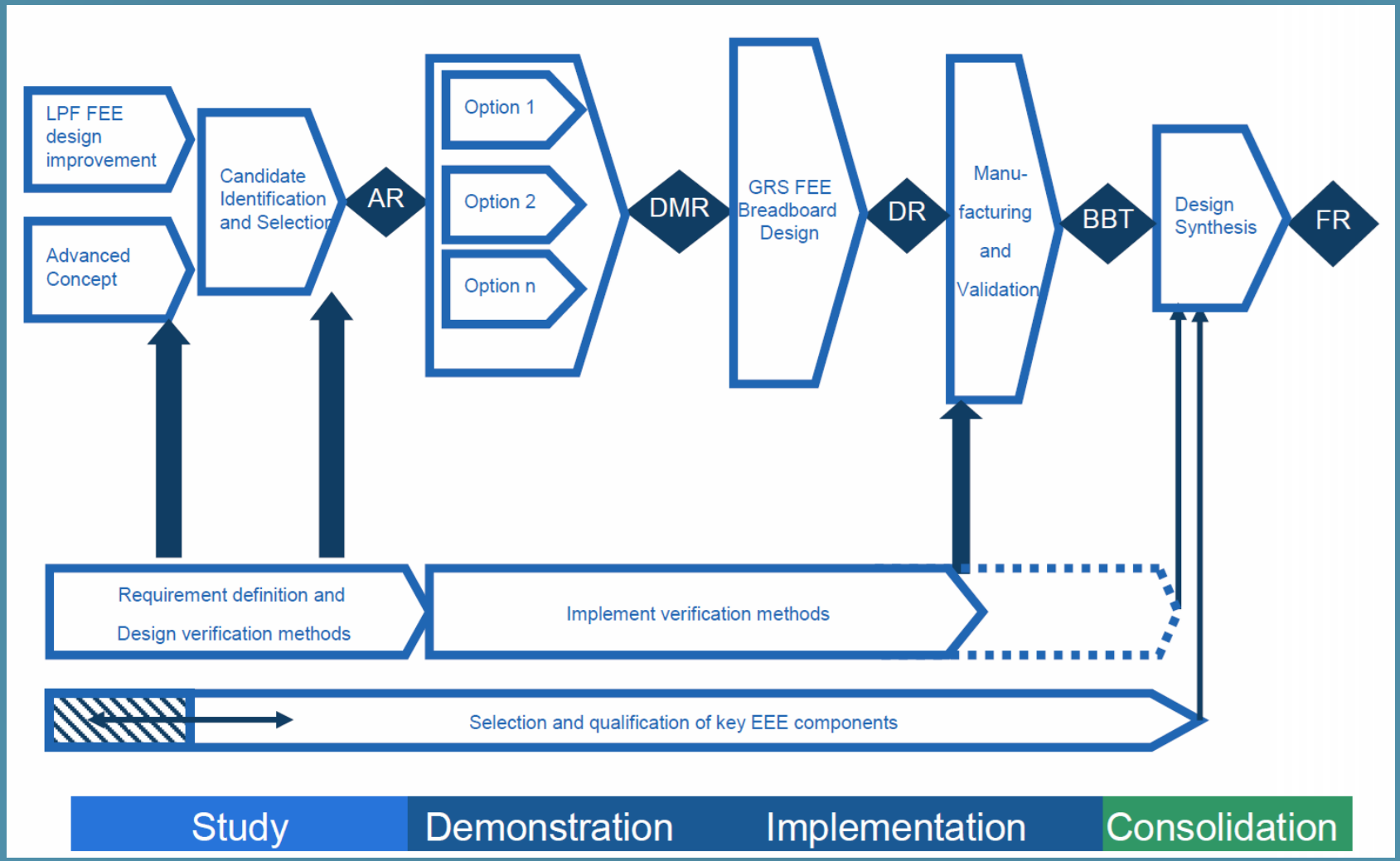
Activity shall

- *assess circuit improvements in order to reach LISA requirements, and assess the key components, such as ADC and DAC, reference voltages and auto-zero amplifiers*
- *identify and test alternatives, if required*
- *revisit the redundancy concept for the LISA design*

Technical roles of the partners in GRS Characterization:

- ***RUAG Space**: Overall project management, system design and integration, digital control electronics, mechanical design, redundancy concept*
- ***HES-SO**: Sensing and actuation electronics*
- ***ETH Zurich**: Requirements, centralized reference voltage,injection voltage generation, tunable test mass simulator and design of test environment*

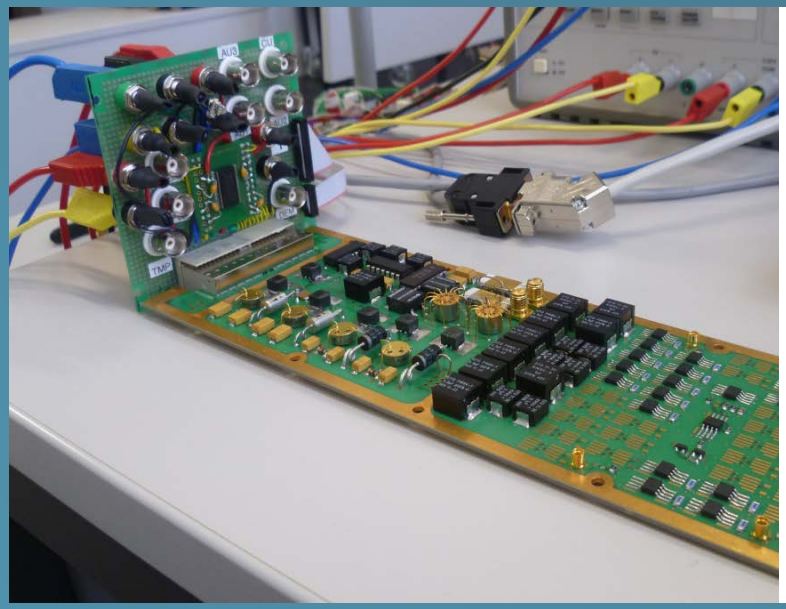
GRS STUDY LOGIC

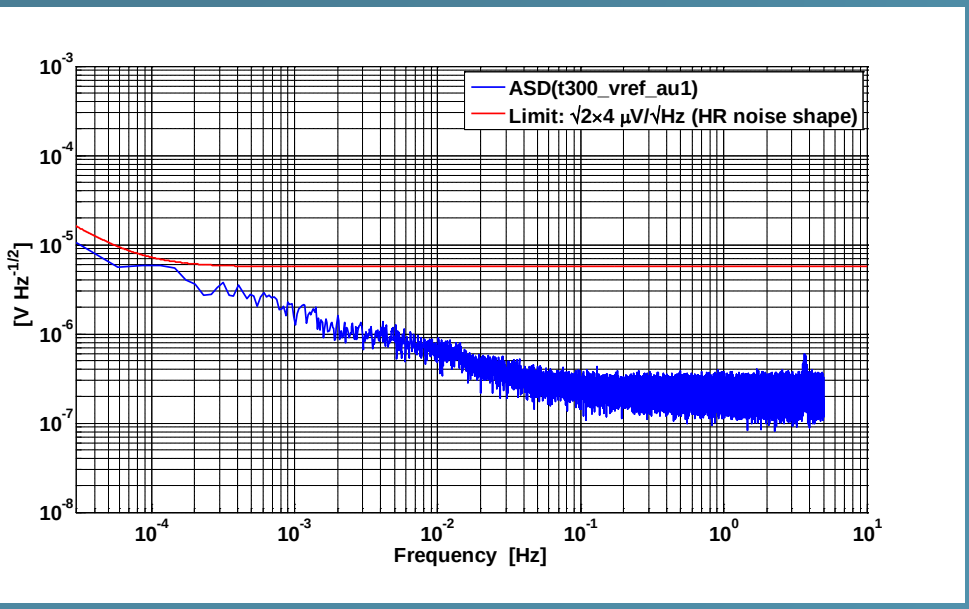


Ultra Stable Voltage Reference - ETH

0.1 mHz to 1 Hz performance range – 1 ppm/√Hz stability

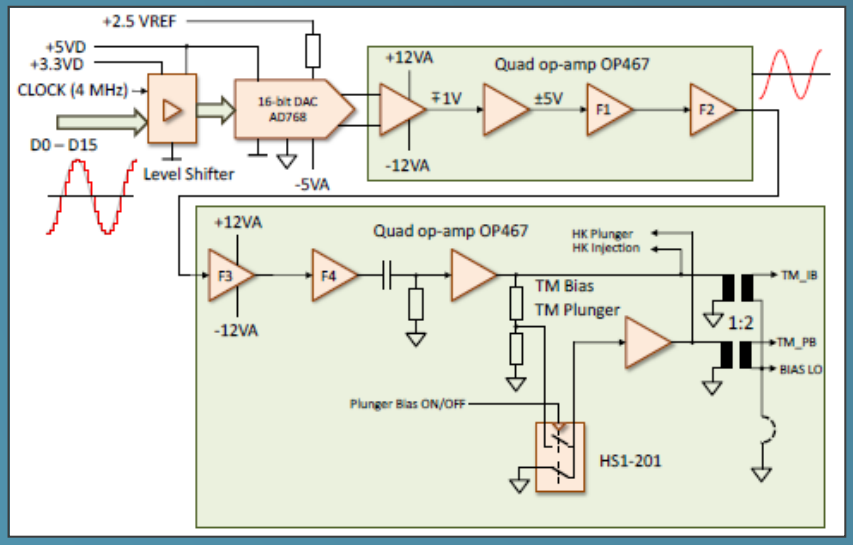
- *Single voltage references have too large noise at low frequency*
- *Solution implemented: combination of multiple references to reduce noise*
- *We combined 20 voltage references (80 was the capability for internal testing) in 4 groups to be able to perform differential measurements*
- *Passive temperature compensation implemented to achieve the sensitivity of 1 ppm/K in the +10 °C to +40 °C FEE operating range*

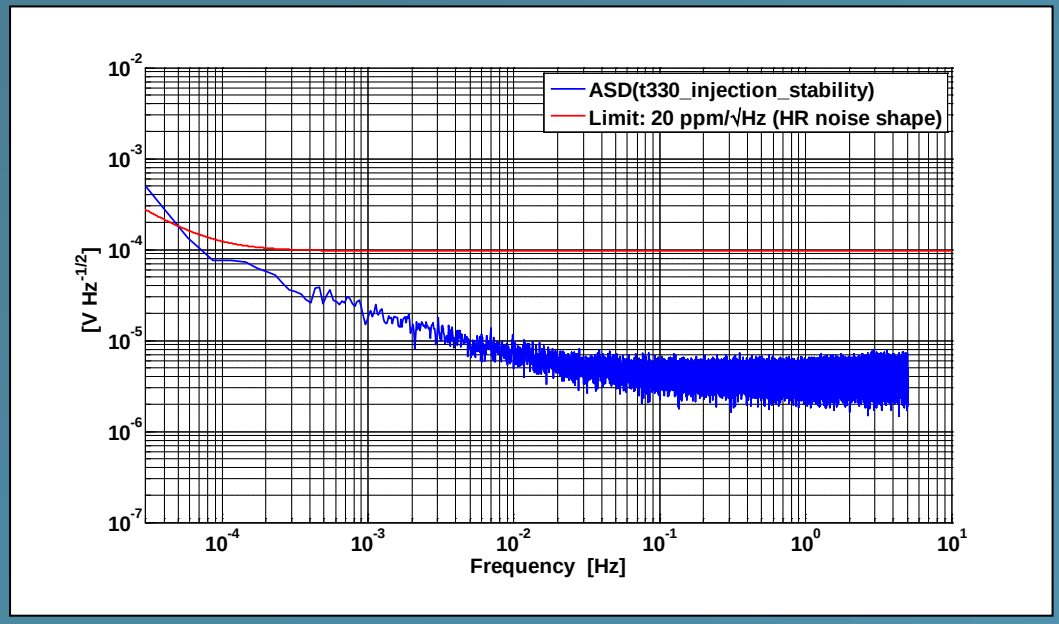




Very Stable Injection Voltage - ETH
0.1 mHz to 1 Hz performance range – 20 ppm/√Hz stability

- *In LTP the injection stability requirement was 50 ppm/sqrtHz*
- *In order to allow a larger alignment range for the laser (±40 µm), a larger sensing performance displacement range and thus a more stringent injection stability was required; injection instability impacts sensing noise*
- *16-bit DAC is generating 100 kHz sine with DAC at 4 MHz sampling*
- *An 8th order low-pass filter removes upper harmonics*





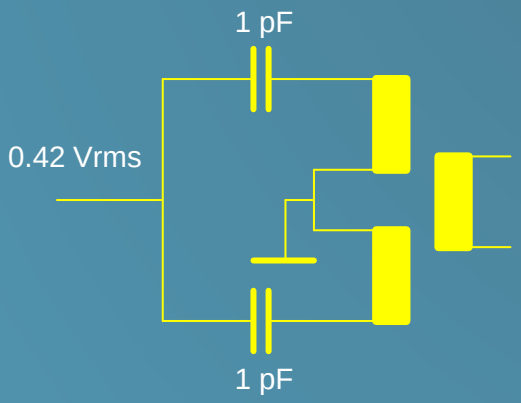
Sensing Circuit – HES-SO

- *Sensing circuit concept remains the same as in LTP (bridge circuit with transformer, TIA, demodulator)*
- *The discrete trans-impedance amplifier (TIA) has been modified to include some gain instead of just buffering the input as in LTP*
- *The demodulator stage has been made with auto-zero amplifiers to cancel the 1/f noise*
- *The central voltage reference (from the ETHZ board) is acquired via differential auto-zero buffer stage to avoid grounding loops*
- *The ADC is driven by an external voltage reference control (since internal circuit generates too large 1/f noise)*
- *A special TM simulator is implemented to reduce influence of stray capacitance for the verification of the sensing performance.*

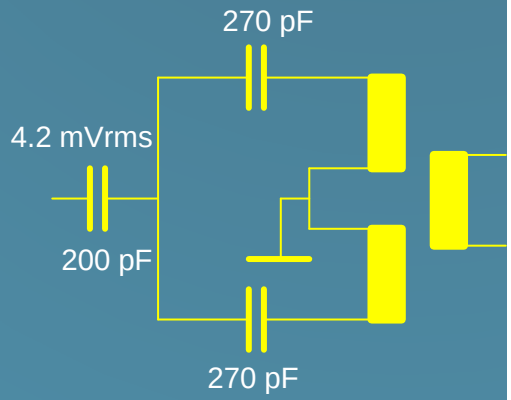
Sensing Noise Measurements – HES-SO

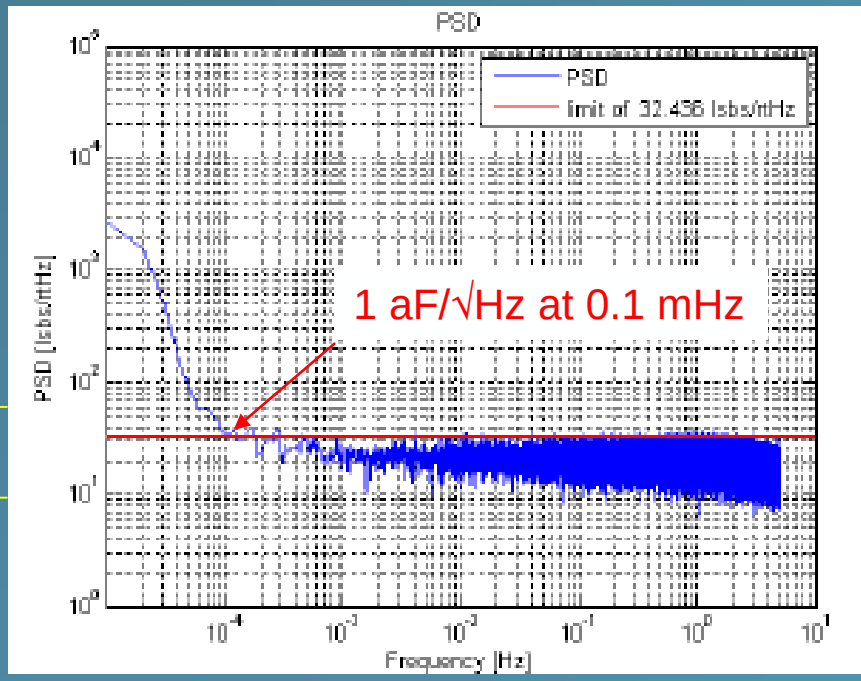
- *Instead of dual 1 pF capacitor simulator a triple capacitor design is implemented using large capacitors*
- *The TM injection level is reduced to maintain the nominal current trough the transformer and the resonance tuning capacitance is adapted to maintain the total required capacitance*
- *The parasitic capacitances now have negligible effect on large simulator capacitors*

TM simulator



TM simulator used for sensing noise verification



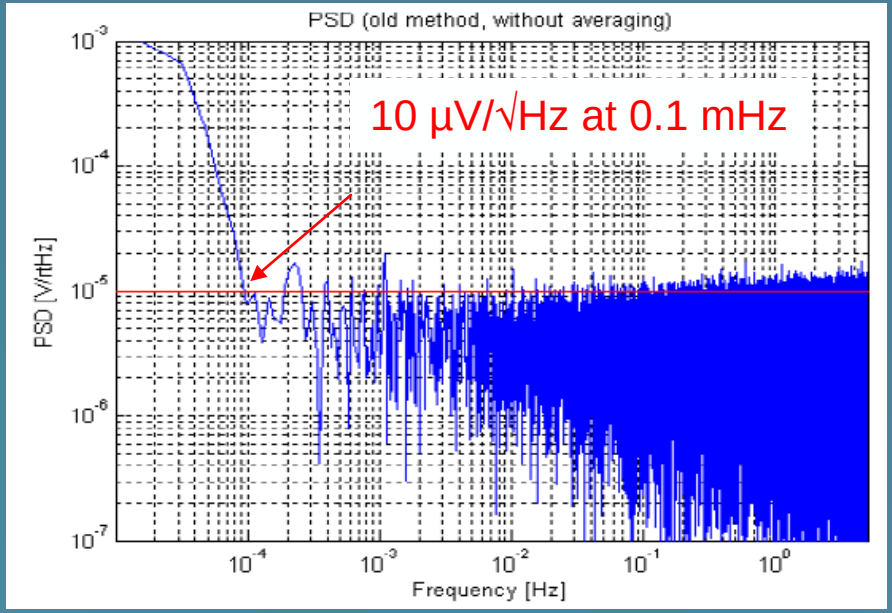


Actuation – HES-SO

- *Central voltage reference , auto-zero buffer stage to decouple grounds*
- *Auto-zero amplifiers are used in the feedback loop to reduce 1/f noise*
- *The ADC in the actuation feedback loop is driven by an external voltage reference control to compensate noise of the reference input circuit*
- *The ADC feedback is equipped with a correlated double sampler, to reject low frequency ADC multiplicative noise.*
- *The digital controller of the sigma-delta loop has larger arithmetic (24bits) to avoid truncation effects as in LTP*
- *The high-voltage amplifier stage is a linear transistor amplifier, to improve the mode switching and start-up behavior (instead of transformer stage and mode switching relays like on LTP; but requires additional ±150 V power lines)*

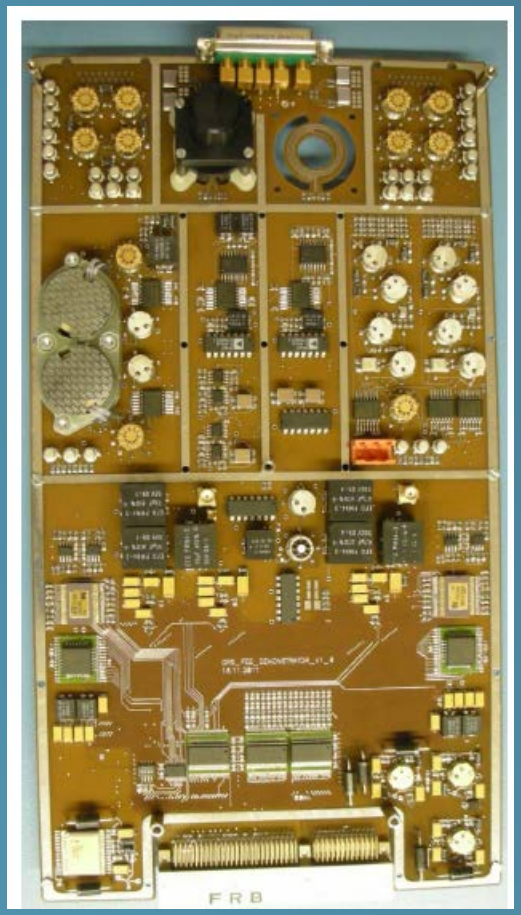
Actuation Noise Measurement – HES-SO

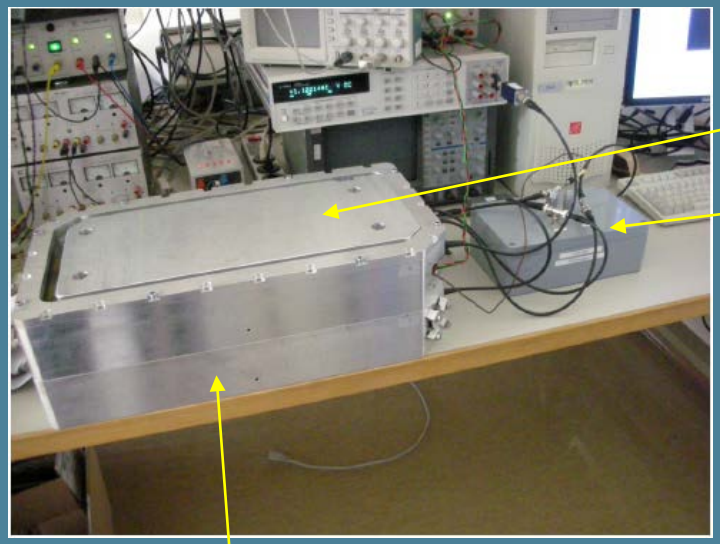
- *Actuation noise measurement performed at 5 V DC output, the required performance was achieved (see chart below)*



- *The actuation amplitude stability could not be measured properly as two boards are needed for uncorrelated differential tests*

Sensing and Actuation Demonstrator – HES-SO





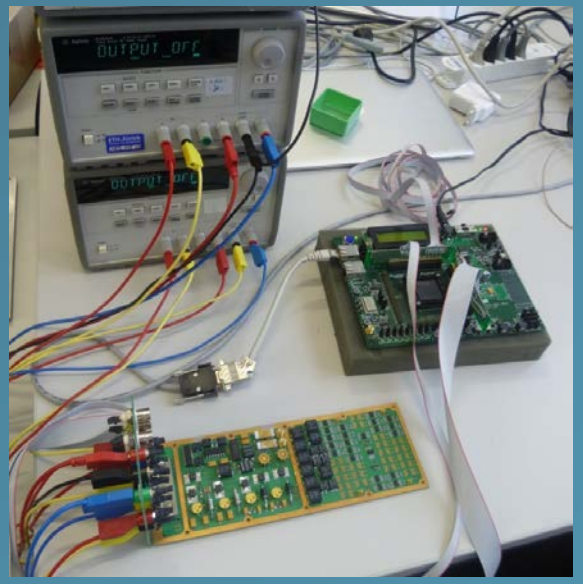
Analog Unit in upper container

TM simulator (old)

Reference Unit
in bottom container

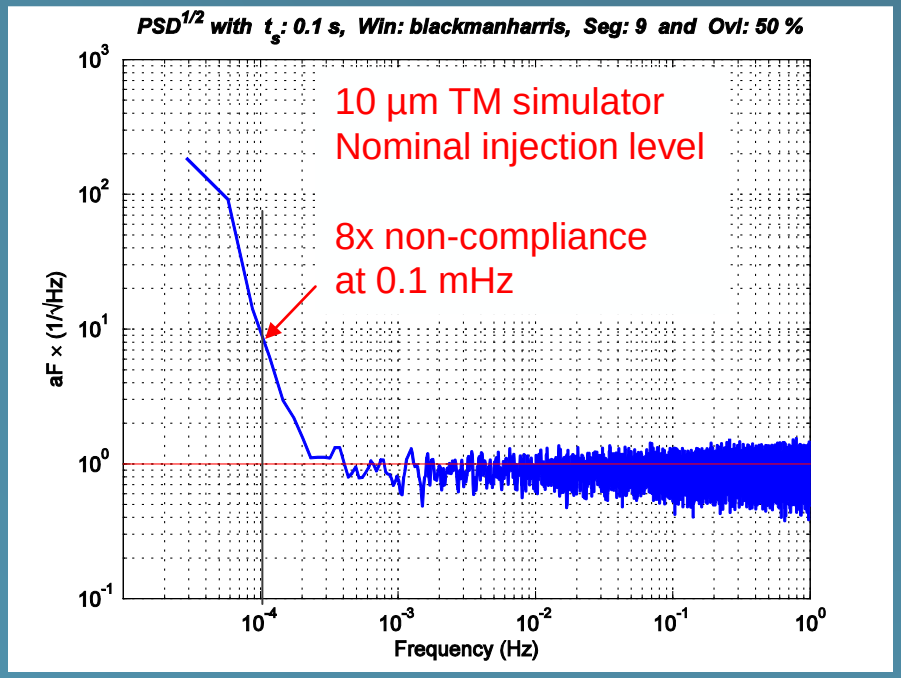
Analog Unit
(sensing and actuation)

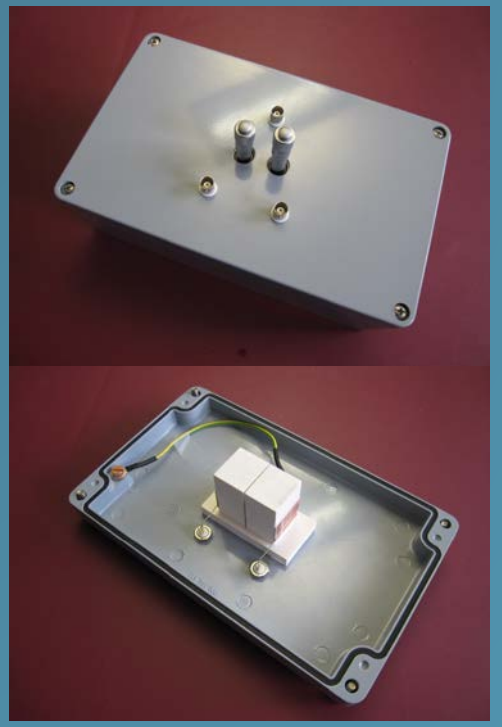
Reference Unit with control EGSE



TM Simulator Measurements – ETH

- *Six TM simulators have been manufactured to allow simultaneous testing of many channels; tuneable from 0 to 120 fF*
- *New test setup had to be developed: a capacitive bridge using two TM simulators and connecting the sensing breadboard such to generate zero common currents through the sensing transformer*
- *Tests were conducted in air, in vacuum and with silica-gel bags*
- *The best result with the ETHZ made sensing breadboard is violating sensing requirement below 0.4 mHz*





GRS PROJECT PHASE 2

- *Implementation of the approved design changes of Phase 1*
- *Manufacturing a GRS FEE BB, consisting of a complete electronics for one TM sensing and control , including redundancy switching, but non-redundant*
- *Upgrade and Verification of the test environment for the BB test campaign*
- *Execution of the test campaign at ETH*
- *Establishment of a Design Synthesis report and recommendations for future models*

- *Approval to proceed for Phase 2 announced*